Amendments

In the specification:

Please substitute the following paragraph for pending paragraph **[0001]**:

--This application is a continuation of Application No. 10/359,201, filed on February 6, 2003, Titled: SUBRANGING ANALOG TO DIGITAL CONVERTER WITH MULTI-PHASE CLOCK TIMING, Inventors: van der GOES et al, which is a continuation of Application No. 10/158,773, filed on May 31, 2002, Titled: SUBRANGING ANALOG TO DIGITAL CONVERTER WITH MULTI-PHASE CLOCK TIMING, Inventors: van der Goes et al., which is a Continuation-in-Part of Application No. 10/153,709, Filed: May 24, 2002, Titled: DISTRIBUTED AVERAGING ANALOG TO DIGITAL CONVERTER TOPOLOGY, Inventors: MULDER et al.; and is related to Application No. 10/158,774, Filed: May 31, 2002, Titled: ANALOG TO DIGITAL CONVERTER WITH INTERPOLATION OF REFERENCE LADDER, Inventors: MULDER et al; Application No. 10/158,595, Filed: May 31, 2002, Titled: HIGH SPEED ANALOG TO DIGITAL CONVERTER, Inventor: Jan MULDER; and Application No. 10/158,193, Filed: May 31, 2002, Inventor: Jan MULDER; Titled: CLASS AB DIGITAL TO ANALOG CONVERTER/LINE DRIVER, Inventors: Jan MULDER et al., all of which are incorporated by reference herein.--

Please insert the following after paragraph **[0024]**:

--FIG. 10 shows the circuit of FIG. 2 with FET transistors used as switches.

FIG. 11 shows cascaded coarse and fine amplifier stages.--

Please substitute the following paragraph **[0028]** for the pending paragraph **[0028]**:

--In one embodiment, 30 coarse amplifiers, 30 coarse comparators, 19 fine amplifiers and 65 fine comparators are used.) The coarse amplifier A_C is connected to a capacitor C_1, which in turn is connected to either the output of a track-and-hold 101, or to V_{coarse} from the reference ladder 104. A two-phase clock, including phases ϕ_1 and ϕ_2, is used to control switches S_1, S_2 and S_3 of the coarse amplifier A_C. When the phase ϕ_1 is on, the switches S_2 and S_3 are closed, the switch S_1 is open. With the switch S_3 closed, the coarse ADC amplifier

A_C is in a reset mode, and the capacitor C_1 is connected to the reference ladder tap V_{coarse}. Also on ϕ_1, the switch S_5 is closed, the switches S_4 and S_6 are open, and the fine capacitor C_2 is connected to an appropriate tap of the reference ladder V_{fine}. Note that all of the switches as S_1-S_6 are typically field effect transistor (FET) switches (see FIG. 10, where the switches are S_1-S_6 illustrated as FET devices). The switch S_3 may be referred to as a coarse ADC reset switch, and the switch S_6 may be referred to as a fine ADC reset switch. When the phase ϕ_1 of the two-phase clock is on, the switches S_3 and S_2 are closed, the amplifier A_C is in a reset mode, and the left side of the capacitor C_1 is connected to a tap of the reference ladder (i.e., V_{coarse}). The switch S_1 is open when ϕ_1 is on.--

Please substitute the following paragraph **[0043]** for the pending paragraph **[0043]**:

-- FIG. 4 further illustrates the operation of the amplifiers of the present invention in a situation where the fine ADC 105 has 4 cascaded stages (typically with a gain of 4x each), which are labeled GA, GB, GC and GD. (See FIG. 11, where two cascaded stages are shown for both fine and coarse amplifiers A_F and A_C, as one example.) In FIG. 4, the amplifier stage of the coarse ADC 102 is labeled GE, the coarse ADC comparator 107 is labeled CC, the fine ADC comparator 108 is labeled FC and the encoder is labeled ENC. The gray portions of FIG. 4 illustrate a progression of one sample's quantization down the amplifier cascade. First, the track-and-hold 101 is connected to the coarse ADC amplifier A_C, during phase ϕ_2. Meanwhile, the coarse comparator 107 (CC) is reset during ϕ_2. The fine ADC amplifier A_F stage GA is also reset. During the next phase ϕ_1, the first stage GA of the fine ADC 105 amplifies, while the second stage GB resets. The process continues, as the signal moves in a pipelined manner down from GA to GB to GC to GD to the fine comparator 108 (FC), and ultimately to the encoder 106. The next quantization is directly behind the quantization just performed, moving from left to right in the figure, and offset by one clock cycle from the measurement illustrated in gray in FIG. 4.--